Applying Complementary Trap Characterization Technique to Crystalline $\gamma$-Phase-$\text{Al}_2\text{O}_3$ for Improved Understanding of Nonvolatile Memory Operation and Reliability

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Abstract—The operation and reliability of nonvolatile memory concepts based on charge storage in nitride layers, such as TANOS (TaN/Al$_2$O$_3$/Si$_3$N$_4$/SiO$_2$/Si), require detailed information on the energy and spatial distribution of the charge defects in both the nitride and the Al$_2$O$_3$ blocking dielectric. This paper focuses on the characterization of Al$_2$O$_3$. We have successfully applied complementary trap characterization techniques to crystalline $\gamma$-phase-Al$_2$O$_3$ in order to obtain a complete picture of the spatial and energetic distribution of the defect density. As a result, two defect types at energy levels 1.8 and 3.5 eV below the conduction band edge are found.

Index Terms—Charge trap (CT) memory, crystalline Al$_2$O$_3$, photodopulation spectroscopy (PDS), TANOS, trap characterization, trap spectroscopy by charge injection and sensing (TSCIS), two-pulse C–V.

I. INTRODUCTION

A GRESSIVE scaling of Flash memory technology, driven by a continuing demand for higher density and lower costs, opens opportunities for charge trap (CT) Flash memory to extend the lifetime of the floating-gate Flash memory to below 30 nm technology nodes [1]. The tunnel oxide in conventional CT Flash however lacks scalability to below 4–5 nm, which leads to a series of shortcomings, e.g., the program/erase window and/or speed at operating voltages.

In contrast to most high-$k$ materials, such as HfO$_2$ [3], [4], ZrO$_2$ [5]–[8], and TiO$_2$ [9], for which higher dielectric constant usually comes at the expense of narrower band gap, typically in the range of 5–6 eV [10], [11] and, consequently, lower barrier heights for electrons and holes, which determine leakage current, Al$_2$O$_3$ has, apart from stable chemical and thermal properties, material characteristics that rank it high in view of application to NVM technologies, e.g., a band gap similar to SiO$_2$, high barrier offset, and a dielectric constant more than double that of SiO$_2$. Consequently, Al$_2$O$_3$ [12], [13] has received considerable attention in the development of nonvolatile memories (NVMs), mainly as replacement for blocking dielectric in TANOS or for IPD in floating-gate cells, where state-of-the-art oxide–nitride–oxide (ONO) stacks lack scalability to below 10 nm [14]. Al$_2$O$_3$ is also interesting in NVM technologies because of the persistence of its insulating properties (e.g., large band gap) after crystallization, which makes it compatible with conventional processes that involve high temperatures above 1000 °C [15]. Unfortunately, Al$_2$O$_3$ has significantly more electron traps, compared with SiO$_2$ [16]–[18], which act detrimentally for NVM reliability. As shown by Mehta et al. [33] using photoinjection–photodopulation, defects are present in the energy range 1.8–3.6 eV below $E_c$ (Al$_2$O$_3$). More recently, Kim et al. [34] showed, using photoconductivity, the existence of two dominant trap levels, located at around 2 and 4 eV below $E_c$ (Al$_2$O$_3$). In this context, it is important to investigate and understand the as-processed and the stress-induced defects in Al$_2$O$_3$. The optimization of Al$_2$O$_3$ and the necessity of overcoming the reliability concerns [19], [20] require a thorough understanding of the distribution of electrical defects.

The aim of this work is to apply complementary trap characterization techniques to crystalline $\gamma$-phase-Al$_2$O$_3$ in order to obtain a complete picture of the spatial and energetic distribution of the defect density. We only aim at characterizing...
the bulk properties of the deposited layers on relatively large areas. For integration into deeply scaled devices, additional processing issues can still modify the defect profiles or induce localize damage. This paper is organized as follows: In Section II, the advantages and drawbacks of each characterization technique are described, along with the sample requirements for each considered techniques. In Section III, we discuss the resulting trap distributions on \( \gamma \)-phase-\( \text{Al}_2\text{O}_3 \) subjected to different thermal treatments, using the techniques described in Section II, and finally, Section IV summarizes the main results.

II. DEVICE AND TECHNIQUE DESCRIPTIONS

A. Devices

The test structures used in this work are MOS capacitors (50 \( \times \) 50 \( \mu \text{m}^2 \)) without junction, as schematized in Fig. 1 and listed in Table I, where a dual-layer \( \text{SiO}_2/\text{Al}_2\text{O}_3 \) stack or a full TANOS stack are used. The thickness of the tunnel oxide of the TANOS stack has been adjusted to provide optimal conditions for controlled charging of the defects in the stack, as it will be explained in Section II. The study of the TANOS structure has been introduced here to account for the structural modifications of the \( \text{Al}_2\text{O}_3 \) layer, which is eventually induced by the nitride charge-trapping film.

The gate stack is deposited on p- or n-type Si substrate and has been manufactured using \textit{in situ} steam-generated (ISSG) oxidation to grow the bottom \( \text{SiO}_2 \) layer. The \( \text{Al}_2\text{O}_3 \) film was deposited by atomic layer deposition (ALD) at 300 \( ^\circ \text{C} \), in a Polygon 8300 chamber, using trimethylysilane, \( \text{Al}([\text{CH}_3])_3 \)-TMA, and \( \text{H}_2\text{O} \) as precursor. A postdeposition anneal (PDA) was carried out immediately after \( \text{Al}_2\text{O}_3 \) deposition and the \( \text{Al}_2\text{O}_3 \) thickness contraction after annealing was accounted for to achieve a target thickness of 10 nm, irrespective of the annealing temperature [21].

All samples received a postannealing treatment, as indicated in Table I. After the gate stack formation, TaN or TiN was deposited using postvapor deposition or 15-nm Au electrodes of 0.5-mm\(^2\) area were evaporated in high vacuum from a resistively heated boat on cold substrate.

B. Techniques

This section describes the complementary and independent (from each other) trap characterization techniques applied to our test structures with crystalline \( \gamma \)-phase-\( \text{Al}_2\text{O}_3 \) in order to obtain a complete picture of the spatial and energetic distribution of the defect density. Note that charge pumping is not included in the list below, since it is mainly an interface characterization technique, while in this paper we aim at characterizing the bulk defects in the \( \text{Al}_2\text{O}_3 \). As shown in [32] charge pumping can scan up to \( \sim 1.2 \) nm and therefore it cannot give additional information in the test structures used in this paper.

1) TSCIS: Trap spectroscopy by charge injection and sensing (TSCIS) has been proposed as a powerful method for characterizing defect bands in dielectric materials [18], [22]. This technique relies on a controlled charging of the \( \text{Al}_2\text{O}_3 \) traps by electrons injected from either the substrate (substrate-side TSCIS, SS-TSCIS) or the gate electrode (gate-side TSCIS; GS-TSCIS) with the charging voltage \( V_{\text{charge}} \) and the charging time \( t_{\text{charge}} \) as measurement parameters.

1) SS-TSCIS uses electron injection from the inversion layer in the substrate at positive \( V_{\text{charge}} \) through a 1-nm \( \text{SiO}_2 \) interface layer separating the substrate from the \( \text{Al}_2\text{O}_3 \) [Fig. 2(b)]. By increasing \( t_{\text{charge}} \) at each \( V_{\text{charge}} \), a trajectory in the dielectric band diagram is defined by the first subband energy level in the inversion layer at the corresponding tunnel distance [Fig. 2(a)]. At low \( V_{\text{charge}} \), the trajectory encompasses only deep traps close to the interface, and with increasing \( V_{\text{charge}} \), the trajectory moves closer to the conduction band edge and further away from the interface, allowing shallow states to be occupied by injected electrons [Fig. 2(a)]. Since \( t_{\text{charge}} \) is mainly a measure of the scanning distance from the substrate interface, thick \( \text{SiO}_2 \) requires longer \( t_{\text{charge}} \) for electrons to tunnel to traps situated in the \( \text{Al}_2\text{O}_3 \) dielectric layer. A \( \text{SiO}_2 \) thinner than 1 nm would, in principle, reduce the charging time even more, but it might however not be deposited reliably. The low \( k \) value of the interface layer has an advantage in that it creates a cantilever effect similar to that of the VARIOT engineered barrier [23] when applying a gate bias \( V_{\text{charge}} \).

Consequently, eventual traps situated in a relatively wide region of the \( \text{Al}_2\text{O}_3 \) band gap may line up in energy with the injection level of the electrons in the inversion layer. These traps may therefore be charged and subsequently electrically probed by SS-TSCIS. Typically, traps between 1.2 and 2.5 eV below \( \text{Al}_2\text{O}_3 \) conduction band (BCB) and up to \( \sim 3 \) nm into the \( \text{Al}_2\text{O}_3 \) can be
observed [24]. In Fig. 2(b), the possible scanning region is indicated by the shaded area.

2) Similar to SS-TSCIS, GS-TSCIS uses electron injection from the metal gate at negative \( V_{\text{charge}} \) and is therefore particularly useful for characterizing defects near the \( \text{Al}_2\text{O}_3/\text{metal} \) gate interface [22]. Note that, in this case, the \( \text{SiO}_2 \) interface layer should be thick enough to avoid parasitic hole injection from or electron discharging to the substrate when applying a negative \( V_{\text{charge}} \). The insulating capability of the interface layer limits the energy scanning range. The thicker the \( \text{SiO}_2 \), the higher the range; therefore, we use samples with 7-nm \( \text{SiO}_2 \) [Fig. 2(c)]. Since a \( \text{Si}_3\text{N}_4 \) layer can be inserted between the interface \( \text{SiO}_2 \) and the \( \text{Al}_2\text{O}_3 \), GS-TSCIS can also be carried out on a full TANOS stack, even with layer thicknesses corresponding to an operational memory stack (4/6/10 nm \( \text{SiO}_2/\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3 \)). The possible scanning region of GS-TSCIS is indicated by the shaded area in Fig. 2(c). Note that, for GS-TSCIS, the scanned energy range is deeper w.r.t. the \( \text{Al}_2\text{O}_3 \) BCB because of the higher band offset of the metal gate, compared with Si. Typically, traps between 2 and 3 eV below the \( \text{Al}_2\text{O}_3 \) BCB at 1.5–2.6 nm from the gate can be observed.

2) PDS: Photodepopulation spectroscopy (PDS) relies on controlled discharging of trapped electrons by photoexcitation with the photon energy as measurement variable [25], [26]. Due to the nature of the experiment, the gate of the device must be transparent to the incident photon flux, and we have used a 15-nm Au gate. At high positive voltage, charging of the \( \text{Al}_2\text{O}_3 \) is achieved by electron tunneling through a 4-nm \( \text{SiO}_2 \) tunneling layer. After charging, the sample is left for several hours in darkness, allowing all shallow traps and traps close to the gate to discharge. Therefore, although the photon energy range for excitation starts from 1.3 eV, electrons trapped at this energy level are not measured, and the effective energy scanning range is narrower, between 2 and 4.5 eV, as indicated in Fig. 3(a) by the shaded area. Note that PDS provides quantitative information on the trap energy levels but is integrated over the occupied part of the spatial profile. The major advantage of this method consists of direct association of the trap photoionization energy to the energy of the exciting photons. Therefore, no oversimplifying assumptions are invoked, allowing the use of the PDS trap distribution as an energy reference for other trap characterization techniques.

3) 2-PCV: Like PDS, two-pulse \( C-V \) (2-PCV) also relies on the controlled discharging of trapped charge, but the discharging is induced by a gate bias allowing electrons to tunnel out of the dielectric as a function of time and applied voltage [27], [28]. Consequently, information on the energy and the spatial distribution of the traps can be extracted. The sample is charged through a \( \text{SiO}_2 \) tunnel oxide, and then, the discharge is monitored as the flatband \( (V_{FB}) \) variation under different conditions. Because of the higher time resolution (\(~\text{ms range}\) range), 2-nm \( \text{SiO}_2 \) provides the optimal balance between minimized measurement time and maximum extracted data. The 2-PCV technique allows extracting entirely quantitative information on the traps in both energy and space, and has the largest scanning range, as indicated by the shaded area in Fig. 3(b).

The difference with the previous techniques is that the spatial and energetic defect profile is not calculated directly from the measured values but is reconstructed from a set of trap parameters that allows fitting the entire measured data set. The physical model is based on first-order detrapping kinetics for monitoring the variation of the charge trapped in the \( \text{Al}_2\text{O}_3 \) stack with time while taking into account possible retrapping due to application of bias during discharging [28]. We have employed 2-PCV to confirm the profile of the traps in both energy and space detected by SS-TSCIS or PDS. Note that 2-PCV requires an n-substrate to avoid parasitic hole injection during the application of negative gate bias for discharging.

4) PPD/PED Technique: In the Post-Program and Post-Erase Discharging (PPD/PED) technique, one measures with high time resolution the evolution of the flatband \( (V_{FB}) \) or threshold \( (V_{TH}) \) voltage immediately after applying a positive \( (V_{PROG}) \) or negative \( (V_{ERASE}) \) voltage pulse. In fact, PPD/PED is a short integrated version of TSCIS with three additional advantages: 1) It does not need dedicated structures with a thin \( \text{SiO}_2 \) interface layer and can be used on any samples. 2) It is significantly less time consuming. 3) It even allows scanning electrons trap below the Si-conduction band. The disadvantage is that all extracted information remains qualitative, and no
deconvolution between energy and space can be carried out. When applied to the memory stack (floating gate or TANOS), PED/PPD provides the transient behavior of a retention characteristic. While retention is a long-term experiment that reveals the charge loss by steady-state leakage mechanisms through tunnel or top oxide layers, PED/PPD reveals only the discharging phenomena in the dielectrics. Since this technique provides qualitative results, we have chosen not to include Al$_2$O$_3$ data in this work. However, all results are consistent, and a detailed overview with various aluminates is presented in [29].

III. TRAP CHARACTERIZATION TECHNIQUES APPLIED TO THE $\Gamma$-PHASE-Al$_2$O$_3$ LAYER

In this section, the complementary trap characterization techniques described in Section II are applied to one particular material: crystalline $\gamma$-phase Al$_2$O$_3$. By combining all experimental results, a complete picture of the spatial and energetic distribution of the defect band structure can be constructed. Due to the long time measurement of most techniques, the
characterization measurements were not performed on a scale to allow statistical analysis of the errors. However, a few repeats were done to check the device variations and the measurement repeatability. Specifically for TSCIS, sample-to-sample, wafer-to-wafer, and lot-to-lot variations were evaluated and shown to be within acceptable margins (~10%).

A. SS-TSCIS

SS-TSCIS is applied to samples S1 (1000 °C N₂) and S2 (1100 °C O₂) listed in Table I. Fig. 4(a) and (b) shows the trap density map versus energy from the top of the Al₂O₃ BCB and distance from the Si/SiO₂ interface, respectively, in samples S1 and S2. Fig. 4(c) and (d) shows the cumulative density plot versus energy, averaged in the Al₂O₃ bulk, together with a Gaussian fit to the main density peak. For both samples, we clearly observe a defect band. These results are fully consistent with trap depth extraction from retention measurements, which predicted a trap band of similar depths to be responsible for retention in floating-gate Flash memory with Al₂O₃ IPD [30].

In S1 (1000 °C N₂), the peak value is fitted at ~1.9 eV and the width (fwhm) = 0.06 ± 0.02 eV. After integration of the Gaussian distribution over energy, we find a bulk Al₂O₃ trap density in the defect band of 1.13 ± 0.02 × 10¹⁹ traps/cm⁻³. In S2 (1100 °C O₂), the peak value is slightly shallower at ~1.65 eV and the width (fwhm) = 0.10 ± 0.02 eV. The corresponding bulk Al₂O₃ trap density after integration is 1.95 ± 0.02 × 10¹⁹ traps/cm⁻³. We also observe an additional concentration of traps below 2 eV for S1 and 1.8 eV for S2. In summary, in sample S2, the defects are more concentrated in a sharply defined defect band, whereas, in sample S1, the defect band is broader, which suggests that O₂ PDA at 1100 °C results in the most complete crystallization of the Al₂O₃, compared with N₂ PDA at 1000 °C. The band in both Fig. 4(a) and (b) is not perfectly horizontal when scanning in the Al₂O₃ bulk, due to either 1) an intermixing of Al₂O₃ with SiO₂ or 2) the presence of a large amount of traps at a deeper level. As we will show in the succeeding sections, a second defect band at deeper level indeed exists and can be charged in a fresh device through the SiO₂ layer that is ~1 nm. Note that the leakage current through shallow defects has strong temperature acceleration, drastically affecting charge loss in memory cells at high temperatures [31].

B. GS-TSCIS

Fig. 5(a) and (b) shows the trap density obtained with GS-TSCIS versus energy from Al₂O₃ BCB and distance from the gate interface, respectively, in samples S3 (1000 °C N₂) and S4 (1100 °C O₂) listed in Table I.
Fig. 5. (a) and (b) Trap density plot versus energy and spatial position using GS-TSCIS on S3 (1000 °C N₂) and S4 (1100 °C O₂) in Table I. (c) Trap density versus depth at a fixed energy level of 3.21 eV from Al₂O₃/BCB, and S4 has a high trap density close to the gate and the steepest drop when scanning further away from the interface. (d) Cumulative density plot versus energy, which is averaged between ∼1.6 and 2 nm from the Al₂O₃/TaN interface for samples S3 and S4. In S3, the trap density drops more gradually and is distributed evenly in both space and energy.

Fig. 5(c) shows the trap density versus depth at a fixed energy of 3.2 eV from Al₂O₃ BCB, and Fig. 5(d) shows the cumulative density plot versus energy, averaged between ∼1.6 and 2 nm from the Al₂O₃/TaN interface. For both samples, a high amount of defects is present at the Al₂O₃/TaN interface. The trap density in S4 (1100 °C O₂) is more concentrated in energy and space, compared with S3 (1000 °C N₂) [Fig. 5(c) and (d)]. Consequently, in S3, a higher density of shallower traps is found.

When erasing a TANOS stack, a dynamic balance is created between trapped electrons in the Al₂O₃ and trapped holes in the nitride. Al₂O₃ traps closer than ∼2 nm from the gate interface are discharged in seconds when applying a small positive voltage (or even 0 V), but traps further away from the metal gate discharge over a very long time period, causing an instability of the $V_{FB}$ versus time, which is known as anomalous erase behavior [22]. The discharging of the bulk Al₂O₃-traps will determine the initial behavior of the retention characteristics from not only the erased state but also the programmed state and should therefore be taken into account when interpreting retention results with Al₂O₃-based blocking dielectrics or IPDs.

C. PDS

PDS is measured on sample S7 (1000 °C N₂). After electron tunneling, Al₂O₃ is found to be charged negatively [cf. initial charge densities in Fig. 6(a)]. This charge is found to be stable when the voltage is swept to either positive or negative values (not shown here), indicating that the electrons are captured by oxide traps. In order to determine the energy depth of these traps, a photoionization experiment is performed to determine the energy distribution of trapped electrons in Al₂O₃, as measured in the energy range of 1.3–4.5 eV below the Al₂O₃ CB. (Fig. 6(b)) Fresh capacitors. (□) Electron injected capacitors. The energy range of trap density determination in the current photoionization experiment extends from 1.3 to 4.5 eV with a maximum at 3.5 eV with a density of state of $1.3 \text{e}^{19} \text{cm}^{-3}$.

Fig. 6. (a) Variation of the oxide charge Q as a function of photon energy in sample S7 (1000 °C N₂) capacitors. The results are shown for fresh (■) and electron-injection (□) samples. (b) The inferred energy distribution of trapped electrons in Al₂O₃, as measured in the energy range of 1.3–4.5 eV below the Al₂O₃ CB. (■) Fresh capacitors. (□) Electron injected capacitors. The energy range of trap depth determination in the current photoionization experiment extends from 1.3 to 4.5 eV with a maximum at 3.5 eV with a density of state of $1.3 \text{e}^{19} \text{cm}^{-3}$. 
were filled upon oxide deposition. The energy of trap depth determined in the current IPE experiment ranges from 1.3 to 4.5 eV with a maximum at 3.5 eV and a trap density of 1.3 e$^{19}$/cm$^{-3}$. More shallow traps are likely to have been emptied at room temperature, because there is no measurable shift of the $C-V$ curve after the first exposure to 1.3-eV photons. This explains why the defects located at $\sim$1.7 eV, as extracted by SS-TSCIS, are not detected here.

The upper limit of the trap energy of the $E_D = 4.5$ eV is determined by the onset of electron IPE from the Si into the CB of the SiO$_2$ tunnel layer. The injected electrons are trapped and compensate for the IPE discharging at $h\nu > 4.5$ eV, leading to the “turn around” in Fig. 6(a).

**D. 2-PCV Technique**

For the samples S8 (1000 °C N$_2$) and S9 (1100 °C O$_2$) listed in Table I, 2-PCV shows the existence of the following: 1) a spatially uniform band of shallow traps and 2) traps concentrated at the SiO$_2$/Al$_2$O$_3$ interface.

1) The shallow trap density peaks at energy $E_D = 1.8$ eV for S8 and at 2 eV for S9 below Al$_2$O$_3$ BCB. The standard deviation is 0.1 eV for both cases, and the energy-integrated trap density is equal to $\sim 1 \times 10^{19}$ cm$^{-3}$ for S8 and $\sim 1.3 \times 10^{19}$ cm$^{-3}$ for S9 [Fig. 7(a) and (b)]. This is consistent with SS-TSCIS and retention measurements.

2) The SiO$_2$/Al$_2$O$_3$ interface traps are normally distributed in two peaks for S8, with one of them distributed between 2.6 and 3.6 eV with a trap density of $3.5 \times 10^{12}$ cm$^{-2}$ at a pick value of 3 eV and the other one distributed between 3.6 and 3.8 eV with a trap density of $2.3 \times 10^{12}$ cm$^{-2}$ at a pick value of 3.7 eV. For S9, the interfacial traps are distributed between 3.2 and 3.7 eV with a trap density of $3 \times 10^{12}$ cm$^{-2}$.

**IV. Conclusion**

We have described and applied different trap characterization techniques on crystalline $\gamma$-phase-Al$_2$O$_3$. SS-TSCIS shows a uniform band of shallow defects at 1.8 eV with a volume density of $1 \times 10^{19}$ cm$^{-3}$ for N$_2$ PDA and 1.65 eV with a volume density of $1.9 \times 10^{19}$ cm$^{-3}$ for O$_2$ PDA. The 2-PCV confirms the existence of this shallow defect band, whereas PDS is insensitive in this energy range. These defects affect strongly the retention of nonvolatile memories with Al2O3 as a blocking layer in TANOS.

GS-TSCIS shows a large peak electron defect density of $1.6 \times 10^{19}$/cm$^{-2}$ at $\sim 3.4$ eV below the Al$_2$O$_3$ BCB close to the gate interface. PDS experiments confirm this trap energy level with an average trap density of $1.3 \times 10^{19}$ cm$^{-3}$, and 2-PCV demonstrates a concentration of defects at the SiO$_2$/Al$_2$O$_3$.
interface at this energy level. When the results of all techniques are combined, it has been concluded that the defect at 3.5 eV is nonuniformly distributed and has its maximum concentration near both Al$_2$O$_3$ interfaces. This defect causes anomalous erase behavior.

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REFERENCES


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